

**Amendments to the claims:**

1 (Presently amended) An apparatus for the downloading  
2 of a code image to a wireless receiver, said apparatus  
3 having:

4 a Sequence Controller generating a ROM controller  
5 enable output and a CPU enable output;

6 a ROM ~~for the storage of~~ having a SRC value, a DST  
7 value, a LENGTH value, and a boot image;

8 a DMA controller ~~responsive to~~ having a SRC register  
9 specifying a source location, a DST register specifying a  
10 destination location, and a LENGTH register, said DMA  
11 controller ~~copying~~ moving an amount of data specified by  
12 said LENGTH register from a said source location specified  
13 by SRC to a said destination location specified by DST for  
14 a duration specified by LENGTH;

15 a ROM controller coupled to said ROM, said ROM  
16 controller initializing said DMA controller upon assertion  
17 of said ROM controller enable output by copying said SRC  
18 value from said ROM to said DMA controller SRC register,  
19 said DST value from said ROM to said DMA controller DST  
20 register, and said LENGTH value from ~~the contents of~~ said  
21 ROM to said DMA controller LENGTH register;

1       a memory coupled to said DMA controller, said DMA  
2 controller copying at least part of said boot image from  
3 said ROM into said memory prior to the assertion of said  
4 CPU enable output; ~~responsive to said DST;~~  
5       a CPU coupled to and executing instructions from said  
6 memory, said CPU enabled upon the assertion of said CPU  
7 enable output;  
8       ~~said CPU enable output asserted after said DMA~~  
9 ~~controller has copied said ROM data to said memory;~~  
10       a wireless front end coupled to said CPU, said CPU  
11 ~~downloading~~ executing instructions from said boot image  
12 causing said cpu to download and execute an operating  
13 system image from a source coupled to a wireless link  
14 accessed through said wireless front end. ~~for use by said~~  
15 ~~CPU.~~

16

17       2(Original) The apparatus of claim 1 where said memory  
18 is a static random access memory.

19

20       3(Original) The apparatus of claim 1 where said memory  
21 is a dynamic random access memory.

22

1           4(Presently amended) The apparatus of claim 2 where  
2   said static random access memory is addressed by said SRC  
3   register.

4

5           5(Original) The apparatus of claim 3 where said CPU  
6   downloads said operating system image into said dynamic  
7   random access memory.

8

9           6(Original) The apparatus of claim 1 where said  
10   sequence controller uniquely asserts said ROM controller  
11   output and said CPU enable output.

12

13           7(Original) The apparatus of claim 1 where said  
14   sequence controller first asserts said ROM controller  
15   output, and asserts said CPU enable output after completion  
16   of copying of said LENGTH from said SRC to said DST.

17

18           8(Original) The apparatus of claim 1 where said boot  
19   image includes instructions for:

20           sending a download request;

21           receiving a packet accompanied by a sequence number;

22           discarding a packet with the same sequence number as  
23   an earlier-received packet;

24           accepting a packet with a unique sequence number;

1           sending a download request if a gap in sequence  
2 numbers is detected.

3

4           9(Original) The apparatus of claim 1 where a download  
5 server with a wireless interface receives a download  
6 request from a wireless client and responds to said  
7 download request by:

8           sending download data including a sequence number,  
9 each download data comprising an original packet and a  
10 duplicate packet each including said sequence number;  
11          incrementing the sequence number for each subsequently  
12 sent download data;

13          upon sending all said download data, thereafter  
14 sending a "done" packet indicating completion of the  
15 download.

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17

18          10(Presently amended) A process for the downloading of  
19 wireless code to a receiver, said process comprising:

20          a first step of copying a SRC value, a DST value, and  
21 a LENGTH value from a ROM to a DMA controller;

22          a second step of said DMA controller copying

23 ~~additional data~~ instructions from said ROM ~~responsive to~~

1 referenced by said SRC ~~address~~ value to a memory ~~responsive~~  
2 location referenced by ~~to~~ said DST value address;  
3 a third step of a CPU executing said instructions  
4 ~~located~~ placed into in said memory by said second step;  
5 a fourth step of said CPU downloading an operating  
6 system program from a remote host using instructions placed  
7 in said memory by said third step, thereafter executing  
8 said operating system program.

9  
10 11(Presently amended) The process of claim 10 where  
11 said SRC ~~address~~ value causes said DMA controller to read  
12 from ~~selects~~ a region in said ROM and said LENGTH defines  
13 a contiguous region of said ROM.

14  
15 12(Presently amended) The process of claim 10 where  
16 said DST value causes said DMA controller to write to  
17 ~~corresponds to an address of~~ a region in said memory.

18  
19 13(Original) The process of claim 10 where said third  
20 step said CPU instructions includes the instructions for:  
21 transmitting a download request;  
22 receiving a packet accompanied by a sequence number;  
23 discarding a packet with the same sequence number as  
24 an earlier-received packet;

1        accepting a packet with a unique sequence number;  
2        sending a download request if a gap in sequence  
3 numbers is detected.

4

5        14(Original) The process of claim 10 where said fourth  
6 step includes:

7        sending a download request;

8        receiving a packet accompanied by a sequence number;

9        discarding a packet with the same sequence number as  
10 an earlier-received packet;

11       accepting a packet with a unique sequence number;

12       sending a download request if a gap in sequence  
13 numbers is detected.

14

15       15(Original) The process of claim 10 where said remote  
16 host responds to said download request by:

17       sending download data including a sequence number,

18 each download data comprising an original packet and a

19 duplicate packet each including said sequence number;

20       incrementing the sequence number for each subsequently  
21 sent download data;

22       upon sending all said download data, thereafter

23 sending a "done" packet indicating completion of the

24 download.

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2       16(Original) The process of claim 15 where said  
3 download data includes an operating system for use by said  
4 CPU.

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6       17(Original) The process of claim 10 where said  
7 original and said duplicate packet are not interleaved.

8

9       18(Original) The process of claim 10 where said  
10 original and said duplicate packet are interleaved.

11

12       19(Original) The process of claim 10 where said  
13 duplicate packet includes a plurality of packets, each said  
14 packet having the same said Tx\_Seq\_Num as said original  
15 packet.

16

17       20-23 Cancelled.

18

19       24 (New claim) An apparatus for the downloading of a  
20 code image to a wireless receiver, said apparatus having:

21       a Sequence Controller generating a ROM controller  
22 enable output and a CPU enable output;

23       a ROM having a SRC value, a DST value, a LENGTH value,  
24 and a boot image;

1           a DMA controller having a SRC register specifying a  
2   source location, a DST register specifying a destination  
3   location, and a LENGTH register, said DMA controller moving  
4   an amount of data specified by said LENGTH register from a  
5   said source location to said destination location;

6           a ROM controller coupled to said ROM, said ROM  
7   controller initializing said DMA controller upon assertion  
8   of said ROM controller enable output by copying said SRC  
9   value from said ROM to said DMA controller SRC register,  
10   said DST value from said ROM to said DMA controller DST  
11   register, and said LENGTH value from said ROM to said DMA  
12   controller LENGTH register;

13          a memory coupled to said DMA controller, said DMA  
14   controller copying at least part of said boot image from  
15   said ROM into said memory;

16          a CPU coupled to said memory, said CPU enabled upon  
17   the assertion of said CPU enable output, said CPU enable  
18   output asserted after said DMA controller has moved said  
19   boot image from said ROM into said memory, said CPU  
20   thereafter executing said boot image from said memory.

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